Author: Ki-Chan(KC) Lee

ISL97687IBZEV1Z Evaluation Board User Guide

The ISL97687IBZEV1Z is a PWM controlled LED driver that supports 4 channels of LED current, for Monitor and TV LCD backlight applications. It is capable of driving 160mA per channel from a 9V to 32V input supply, with current sources rated up to 75V absolute maximum. Figure 1 shows a photo of a 14 LED/Channel with a 120mA/Channel. The ISL97687IBZEV1Z in Figure 2 is designed for a one layer PCB with SOIC package.

Quick Start Guide

1. The ISL97687 provides many different PWM dimming methods; the interface modes and its settings are summarized in Table 2. Those interfaces can be selected with switches and jumper settings of the ISL97687IBZEV1Z evaluation board in Figures 2 and 4.

   a. **Direct PWM Dimming Mode**
   Connect jumper on right pin and middle pin of the JP_PWM_SET by applying VDC to PWM_SET/PLL pin. In this mode, all other inputs (ACTL, STV , EN_PS, EN_VSYNC, EN_ADIM) will be neglected. The LED dimming frequecy and phase of the LEDs will be the same as the input of PWMI, as shown in Figures 5 and 6.

   b. **Decoded PWM Dimming Mode**
   Connect jumper of middle and left pin on the JP_PWM_SET by applying POT resistor of R_PWM_SET to adjust LED dimming frequency, as shown in Figures 7 and 8. The JP_CPLL should be opened.

   c. **VSYNC Mode**
   Connect jumper to the JP_CPLL and remove the jumper of the JP_PWM_SET. Set switch SW_EN_VSYNC to be ON(H). The LED dimming frequency will be selected by frame signal coming to the STV pin (see Table 1 in the ISL97687 datasheet). Figures 9 and 10 show the STV and channel output waveforms at VSYNC mode.

   d. **Phase Shift Mode**
   Connect Jumper to the JP_PWM_SET for decoded PWM dimming mode or JP_CPLL for VSYNC mode. Set the switch SW_EN_PS to be ON(H) state. Figure 8 shows phase shifted channel output. Figure 10 shows the channel output waveforms in the phase shifted VSYNC mode.

   e. **ACTL Interface mode**
   Connect jumper JP_PWM_SET for decoded PWM dimming mode or JP_CPLL for VSYNC mode. Set switch SW_EN_ADIM to ON state. Apply analog control signal 0.3V(0% dimming) ~ 3.0V(100% dimming) to the ACTL post (see Figure 5). In the ACTL or ACTL*PWMI mode, the PWMI pin should not be floating or GND but tied to VDC or applying PWM signal.

2. The ISL97687IBZEV1Z evaluation board provides the adjustments of Boost switching frequency, LED dimming frequency, and LED peak with jumpers and potentiometers, as shown in Figure 4. Follow the steps for the adjustment and selection of the analog settings.

   a. **Boost switching frequency adjustment**
   Change the resistance of the potentiometer R_OSC for the boost switching frequency adjustment.

   b. **Dimming frequency adjustment**
   Place jump JP_PWM_SET between middle and left pins to connect PWM_SET pin to the potentiometer for the dimming frequency adjustment.

   c. **LED peak current adjustment**
   For two step LED peak current settings, setup the current levels with potentiometer of R_ISET1 and R_ISET2 of fixed resistor R16 (36.5kΩ populated for 80mA). The required current levels can be selected with switch SW_CSEL.

   d. **OVP threshold setting**
   The OVP level can be set based on Equation 1. The boost can regulate down to 30% of OVP. The OVP level should be considered max forward voltage of strings and margin of low temperature start-up.

   $$OVP = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad \text{(EQ. 1)}$$

   Please refer to the ISL97687 datasheet for detailed switching and regulation adjustment.

3. For power-up, set switch SW_nSHUT to right side position. Apply input supply voltage to the PVIN and PGND pins based on the load conditions according to Table 1.

4. Each LED string can be connected to the posts of CH1, CH2, CH3, and CH4 with VOUT bias to the combined anodes. The Max LEDs per strings can be up to 22 LEDs for 79.3V OVP. Make sure the minimum number of LEDs/string will be limited by 30% (23.8V) of Boost OVP level.

TABLE 1. LOAD CONDITION OF ISL97687 EVALUATION BOARD

EVALUATION BOARD ISL97687IBZEV1Z	
Max LEDs/Ch	Driving up to 22 LEDs/Ch
OVP limit	79.3V (23.8V of 30% OVP)
Current limit	4.25A (sense resistor 40mΩ)
Typical input voltage range I	20V to 30V for 12 to 22 LEDs with 120mA/Ch
Typical input voltage range II	10V to 20V for 10 to 14 LEDs with 120mA/Ch

NOTE: Input voltage range, number of LEDs/Ch, and LED peak current can be adjusted by the current sense and OVP settings but needs careful attention on the Abs rating of the components.

Photographs of ISL97687IBZEV1Z Setup and Board

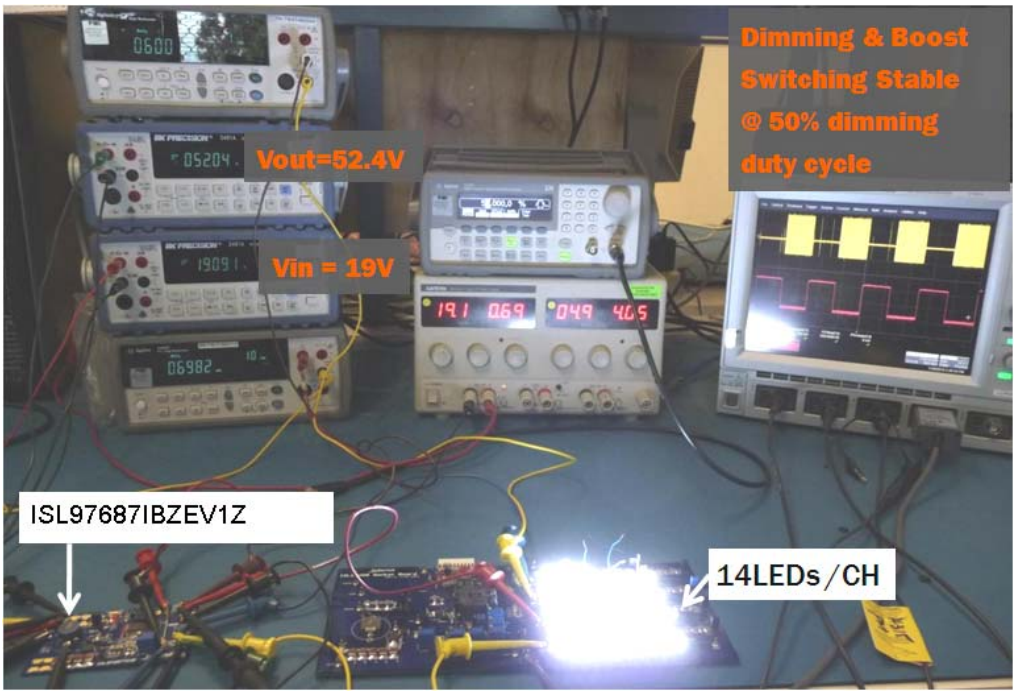

FIGURE 1. PHOTO OF ISL97687IBZEV1Z DRIVING SETUP

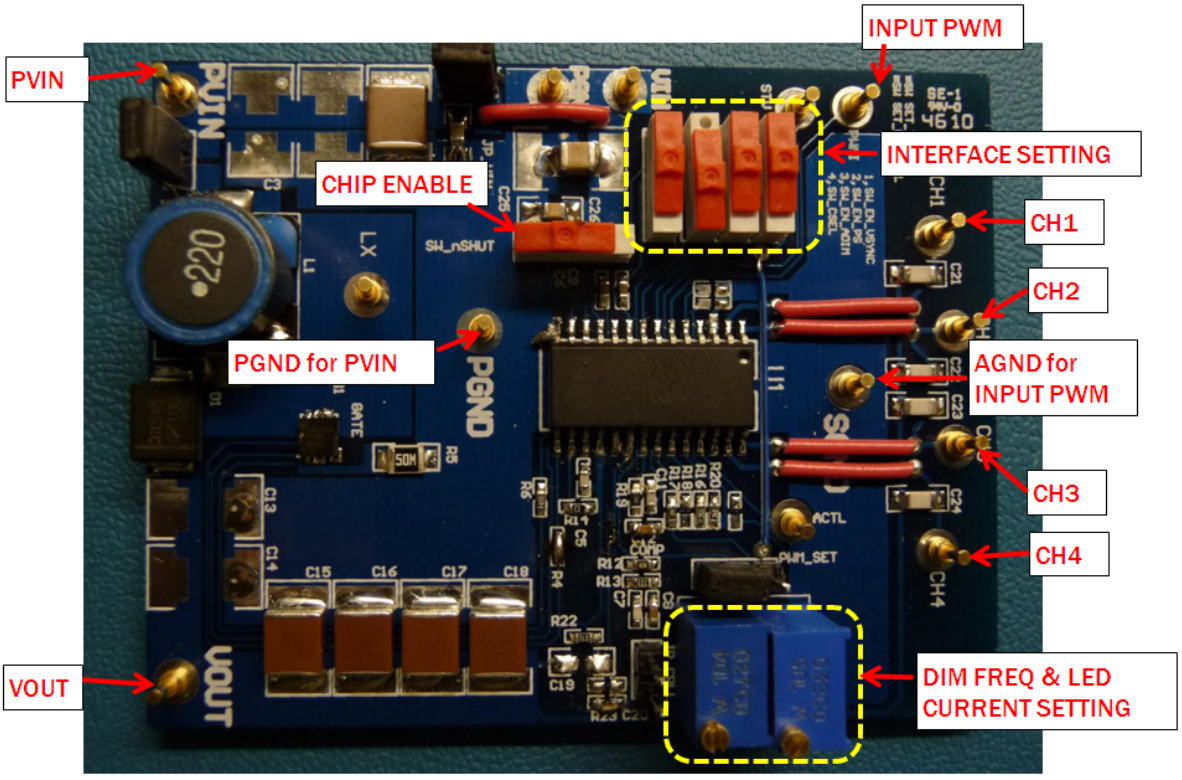

FIGURE 2. PHOTO OF ISL97687IBZEV1Z DESIGNED FOR 1-LAYER PCB

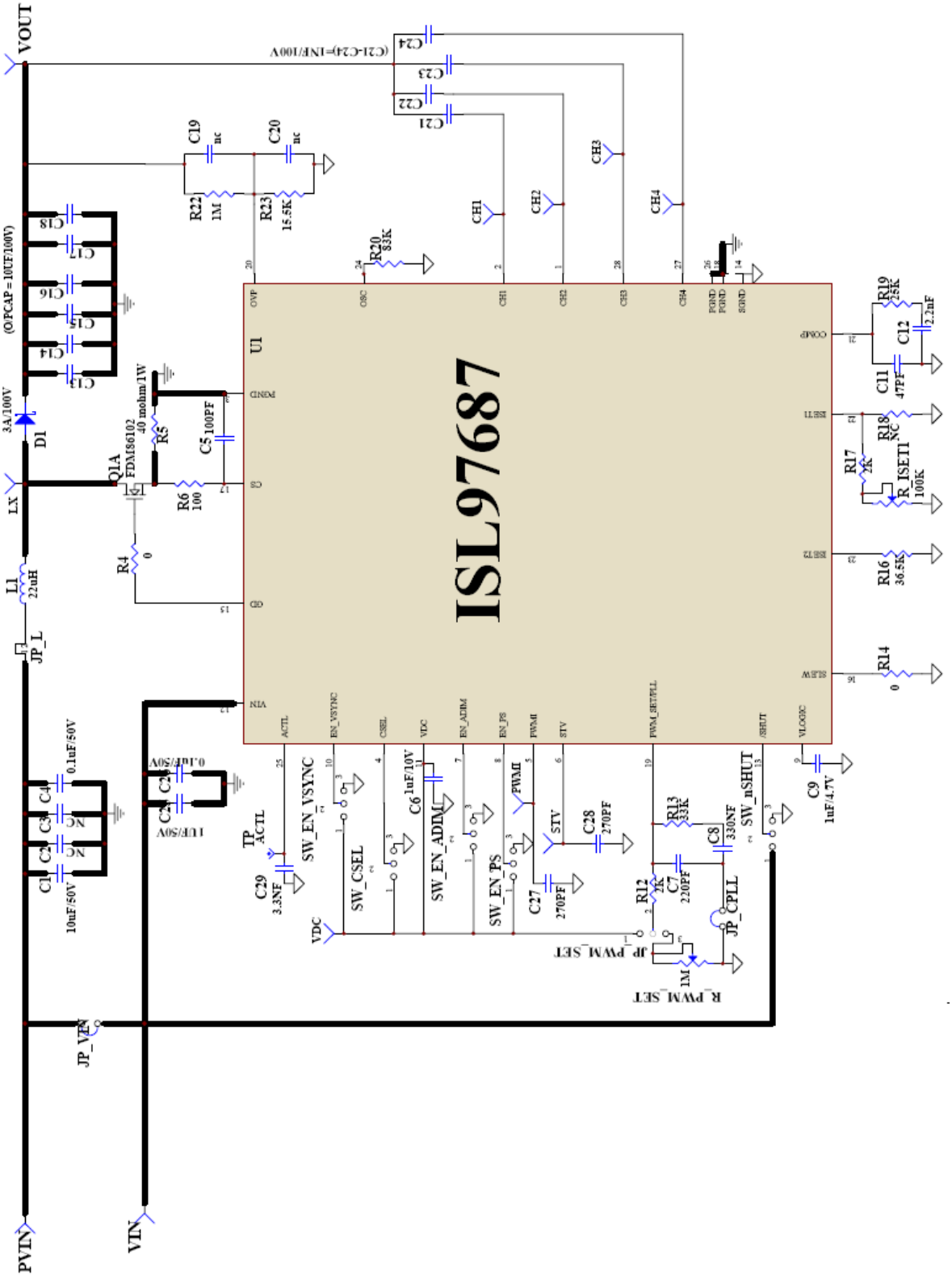

FIGURE 3. ISL97687IBZEV1Z SCHEMATIC

TABLE 2. SWITCH SETTINGS FOR INTERFACE MODE SELECTION

Interface mode	Input signal and component connection to the pin						
	JP_PWM_SET /PLL	PWMI	ACTL	STV	EN_ADIM	EN_VSYNC	EN_PS
Direct PWM dimming mode	H	Y	N	N	N	N	N
Decoded PWM dimming mode only	Resistor connection for dimming freq adjustment	Y	N	N	L	L	L
VSYNC mode	RC loop filter for PLL	Y	Y	Y	Y	H	Y
Phase shift mode	Resistor connection for dimming freq adjustment or RC loop filter for VSYNC	Y	Y	Y	Y	Y	H
ACTL mode	Resistor connection for dimming freq adjustment or RC loop filter for VSYNC	H	Y	Y	H	Y	Y
ACTL * PWMI mode	Resistor connection for dimming freq adjustment or RC loop filter for VSYNC	Y	Y	Y	H	Y	Y

H: Tied to VDC
L: Tied to GND

Y: Input signal available or mode selectable
N: Input signal not available or negligible

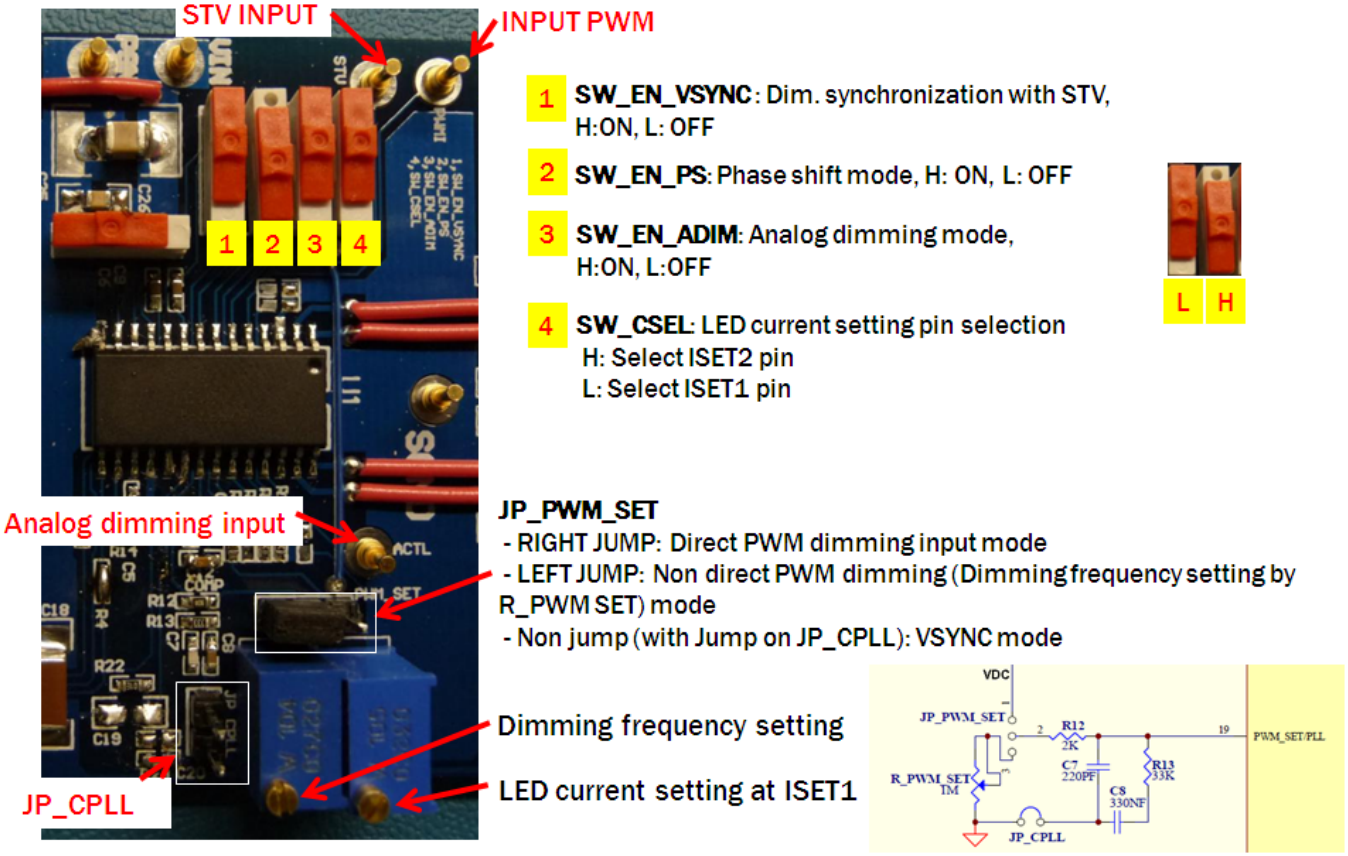

FIGURE 4. JUMPER SETTINGS FOR INTERFACE MODE, DIMMING CURRENT AND FREQUENCY ADJUSTMENT

Waveforms

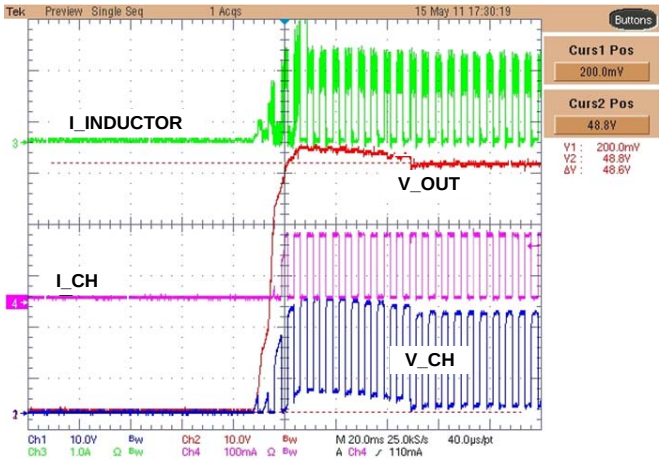

FIGURE 5. START-UP (DIRECT PWM DIMMING, V_{IN}: 19V, I_{CH}: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

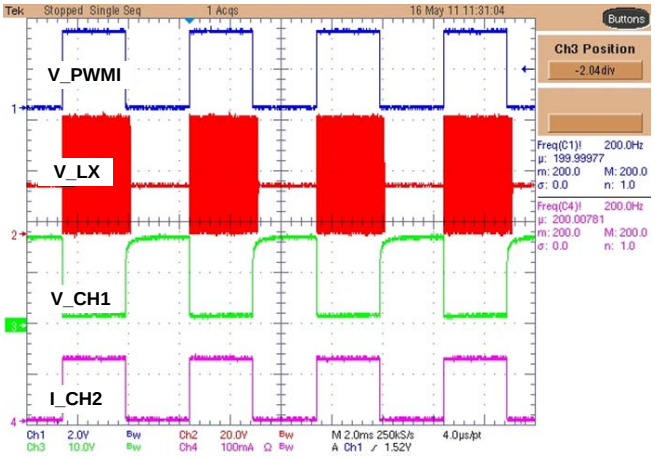

FIGURE 6. DIRECT PWM DIMMING (V_{IN}: 19V, LEDs: 4P18S, f_{DIM}: 200Hz)

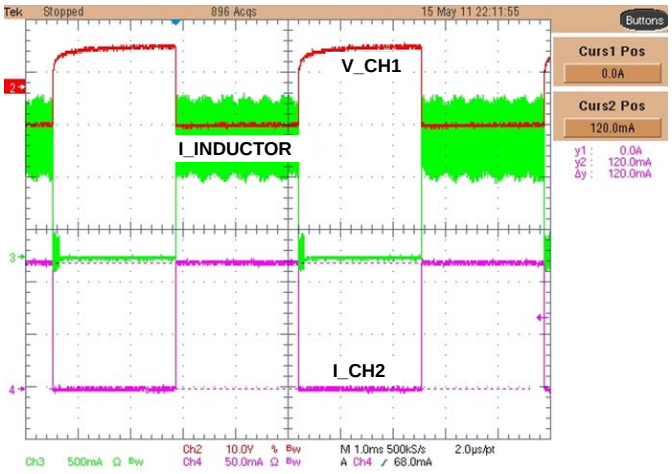

FIGURE 7. PWM DIMMING WITHOUT PHASE SHIFT (V_{IN}: 19V, ICH: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

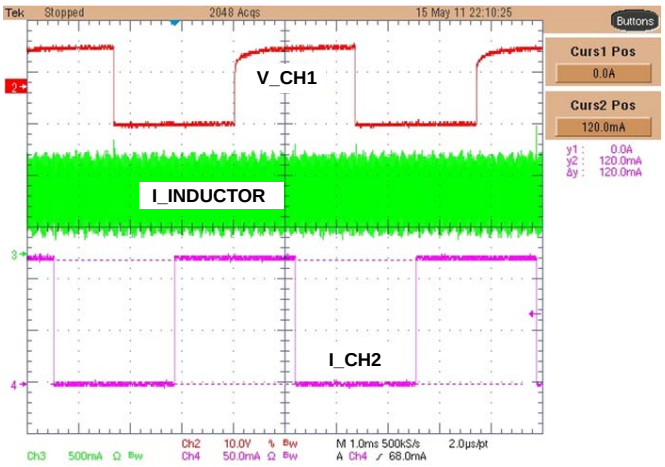

FIGURE 8. PWM DIMMING WITH PHASE SHIFT (V_{IN}: 19V, ICH: 120mA, LEDs: 4P18S, f_{DIM}: 200Hz)

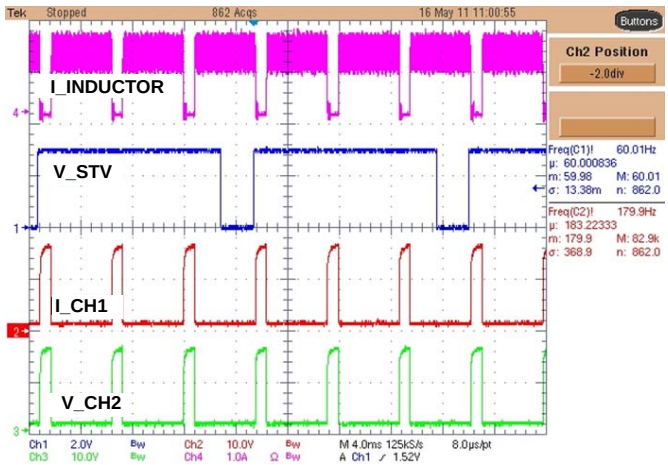

FIGURE 9. VSYNC ENABLED DIMMING WITHOUT PHASE SHIFT (VIN: 19V, ICH: 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)

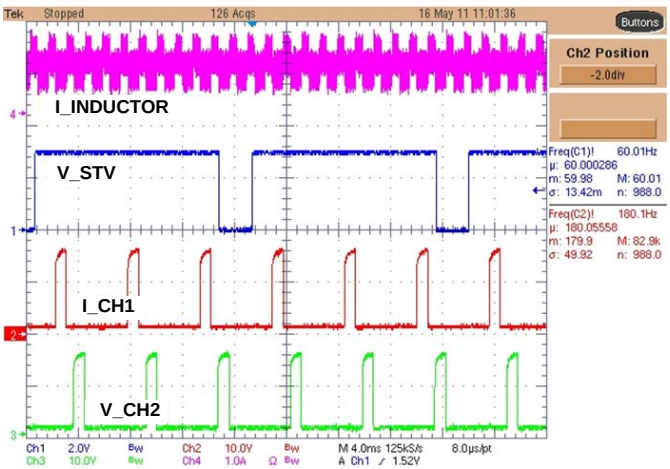

FIGURE 10. VSYNC ENABLED WITH PHASE SHIFT (V_{IN}: 19V, ICH: 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)

One Layer PCB Layout With SOIC Package

This type of layout is particularly important for this type of product, as the ISL97687 has a high power boost, resulting in high current flow in the main loop's traces. Careful attention should be focused in the following layout details:

1. Boost input capacitors, output capacitors, inductor and Schottky diode should be placed together in a nice tight layout. It is important to keep the nodes closely coupled by keeping the grounds of the input, output, ISL97687 and the current sense resistor connected with a low impedance and wide metal .
2. If possible, try to maintain central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. The filtering capacitors should be placed close to the VIN pin.
3. For optimum load regulation and true V_{OUT} sensing, the OVP resistors should be connected independently to the top of the output capacitors and away from the higher dv/dt traces. The OVP connection needs to be as short as possible to the pin. The AGND connection of the lower OVP components is critical for good regulation. At 70V output, a 100mV change at V_{OUT} translates to a 1.7mV change at OVP. Thus, a small ground error due to high current flow (if referenced to PGND) can be disastrous.
4. The bypass capacitors connected to VDC and VLOGIC need to be as close to the pin as possible, and again should be referenced to AGND. This is also true for the COMP network and the rest of the analog components (on ISET1/2, PWM_SET, etc.).
5. The inductor and input and output capacitors should be mounted as tight as possible, to reduce the audible noise and inductive ringing.

The general rules for a two layer PCB layout can be applied to the one layer PCB layout of the SOIC package, although this layout is much more challenging and very easy to get wrong. The noisy PGND of the switching FET area and quiet AGND must be placed on the same plane as shown in Figure 11, therefore, great care must be taken to maintain a stable and clean operation, due to increased risk of noise injection to the quiet area.

1. The GND plane should be extended as far as possible as space allows to spread out heat dissipation.
2. All ground pads for input caps, current sensor and output caps should be close to the PGND pin adjacent to the CS pin of ISL97687 with wide metal connection shown in Figure 11. This guarantees a low differential voltage between these critical points.
3. The connection point between AGND pin 14 and PGND pin 18 should be " Narrow" neck, effectively making a star ground at the AGND pin.
4. The relatively quiet AGND area to the right of the neck needs to be traced out carefully in unbroken metal (via the shortest possible path) to the ground side of the components connected to OVP, COMP, ISET, ACTL, PWM_SET/PLL, and ACTL. This is also true for the filtering caps on PWMI and STV. These are needed to reject noise and cause decoding errors in some conditions.
5. The current sensing line is shielded by a metal trace, coming from its source, to prevent pickup from the GND pin beside it.
6. The filtering cap of the current sensing line should be placed close to the CS pin rather than in the area of current sense resistor, as it needs to couple this pin to the adjacent PGND pin.
7. The noisy switching FET should be kept far away from the quiet pin area.
8. The area on the switching node should be determined by the dissipation requirements of the boost power FET.

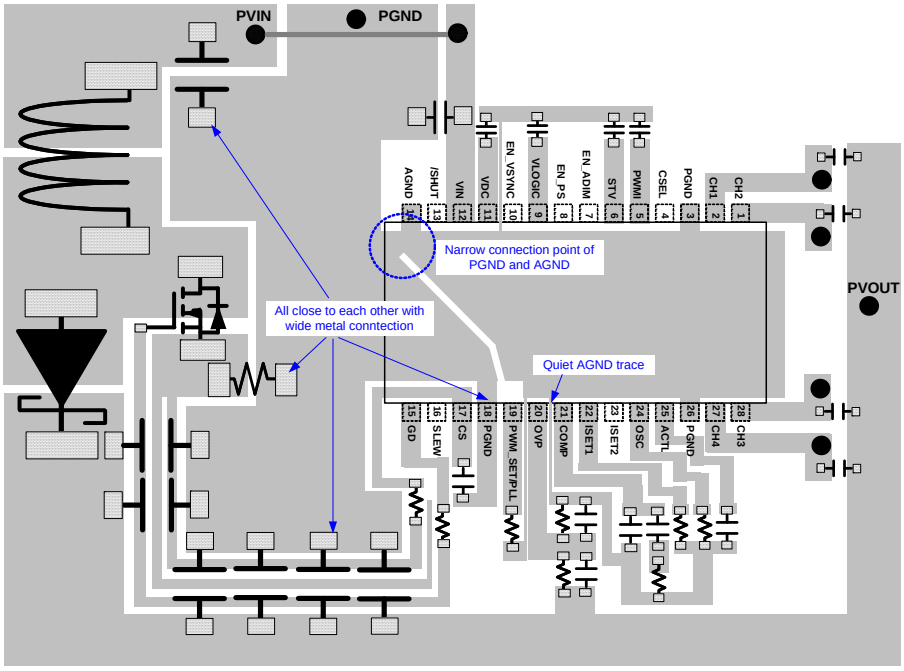

FIGURE 11. EXAMPLE OF ONE LAYER PCB LAYOUT

Bill of Materials

PART TYPE	DESIGNATOR	FOOTPRINT
0	R4	603
0	R14	603
0.1µF/50V	C4	C4
0.1µF/50V	C26	C4
1M	R22	603
1M	R_PWM_SET	VRES
1nF/100V	C24	C4
1µF/50V	C25	C1_C3
1nF/100V	C21	C4
1nF/100V	C23	C4
1nF/100V	C22	C4
1µF/4.7V	C9	603
1µF/10V	C6	603
2.2nF	C12	603
2k	R12	603
2k	R17	603
3.3nF	C29	603
3A/100V	D1	DO-403A
NC	C20	603
10µF/50V	C1	C1_C3
10µF/100V	C17	C13_C18
10µF/100V	C14	C13_C18
10µF/100V	C13	C13_C18
10µF/100V	C18	C13_C18
10µH	L1	10µH/5.1A
15.5k	R23	603
40mΩ/1W	R5	1206
25k	R19	603
33k	R13	603

PART TYPE	DESIGNATOR	FOOTPRINT
ACTL	TP	TESTPOINT
AGND	J17	POWERPOST
AGND	J18	POWERPOST
AGND	J16	POWERPOST
AGND	J15	POWERPOST
CH1	J9	POWERPOST
CH2	J10	POWERPOST
CH3	J11	POWERPOST
CH4	J12	POWERPOST
FDM86102	Q1	FDM86102
ISL97687	U1	SOIC28
JUMPER-3PIN	JP_PWM_SET	JUMPER-3PIN
JUMPER	JP_CPLL	JUMPER-2PIN
LX	J3	POWERPOST
NC	R18	603
NC	C2	C1_C3
NC	C3	C1_C3
NC	C15	C13_C18
NC	C16	C13_C18
PGND	J13	POWERPOST
PGND	J14	POWERPOST
PVIN	J2	POWERPOST
PWMI	J8	POWERPOST
STV	J20	POWERPOST
SWITCH	SW_EN_ADIM	SWITCH-SLIDE-SPDT
SWITCH	SW_EN_PS	SWITCH-SLIDE-SPDT
SWITCH	SW_CSEL	SWITCH-SLIDE-SPDT
SWITCH	SW_EN_VSYNC	SWITCH-SLIDE-SPDT
SWITCH	SW_nSHUT	SWITCH-SLIDE-SPDT

Bill of Materials (Continued)

PART TYPE	DESIGNATOR	FOOTPRINT
36.5k	R16	603
47pF	C11	603
83k	R20	603
100	R6	603
100k	R_ISET1	VRES
100pF	C5	603
NC	C19	C19
220pF	C7	603
270pF	C27	603
270pF	C28	603

PART TYPE	DESIGNATOR	FOOTPRINT
VDC	J5	POWERPOST
VIN	J1	POWERPOST
VOUT	J4	POWERPOST
WR	JP_L	JUMPER-2PIN
330nF	C8	603